Analog Power AM4536C

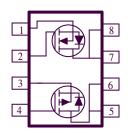
P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY				
$V_{DS}(V)$	$r_{DS(on)} m(\Omega)$	$I_{D}(A)$		
30	$42 @ V_{GS} = 4.5V$	5.8		
30	$28 @ V_{GS} = 10V$	7.1		
-30	$59 @ V_{GS} = -4.5V$	-4.9		
	39 @ V _{GS} = -10V	-6.0		

- $\hbox{ Low $r_{DS(on)}$ provides higher efficiency and} \\ \hbox{ extends battery life}$
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology





ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)							
Parameter			N-Channel	P-Channel	Units		
Drain-Source Voltage		V_{DS}	30	-30	V		
Gate-Source Voltage			±20	±20	V		
Continuous Drain Current ^a	T _A =25°C	T_	7.1	-6.0			
Continuous Drain Current	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	ΙD	5.8	-4.9	Α		
Pulsed Drain Current ^b		I_{DM}	20	-20			
Continuous Source Current (Diode Conduction) ^a			1.3	-1.3	A		
D D a	T _A =25°C	D	2.1	2.1	W		
Power Dissipation ^a	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	I D	1.3	1.3	VV		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Maximum Units				
N	t <= 10 sec	D	62.5	°C/W		
Maximum Junction-to-Ambient ^a	Steady State	$R_{ heta JA}$	110	°C/W		

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

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D	g , ,	T C 142	Limits				TT *4
Parameter	Symbol	Test Conditions	Ch	Min	Typ	Max	Unit
Static							
Gate-Threshold Voltage	V	$V_{GS} = V_{DS}$, $I_D = 250 \text{ uA}$	N	1			v
Gate-Timeshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = -250 \text{ uA}$	P	-1.0			•
Gate-Body Leakage	I_{GSS}	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$	P N			±100 ±100	nA uA
	055	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$ $V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$	P	\vdash		-1	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	N			1	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 0 \text{ V}$	N	20			Α
On-State Drain Current	1D(on)	$V_{DS} = -5 \text{ V}, V_{CS} = -10 \text{ V}$	P	-20			А
		VGS = 10 V, ID = 7.1 A	N			28 42	
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$VGS = 4.5 \text{ V}, I_D = 5.8 \text{ A}$ $VGS = -10 \text{ V}, I_D = -6 \text{ A}$	_				mΩ
		VGS = -4.5 V. ID = -4.9 A	P			59	
Forward Tranconductance ^A	g_{fs}	$V_{DS} = 15 \text{ V}, I_{D} = 6.9 \text{ A}$ $V_{DS} = -15 \text{ V}, I_{D} = -5.2 \text{ A}$	N		25		S
	&IS	$V_{DS} = -15 \text{ V}, I_{D} = -5.2 \text{ A}$	P		10		J
Dynamic							
Total Gate Charge	Q_{g}	N-Channel	N		4.0		
		$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 6.9 \text{ A}$	P N		10		
Gate-Source Charge	Q_{gs}	P-Channel	P		2.2		nC
G. D. G		V _{DS} =-15V, V _{GS} =-10V, I _D =-5.2A	N		1.4		
Gate-Drain Charge	Q_{gd}	VDS= 13 V, VGS= 10 V, ID= 3.211	P		1.7		1
Turn On Dalay Time	+	, i i i i i i i i i i i i i i i i i i i		8			
Гurn-On Delay Time	td(on)		10		[
Rise Time	t _r	$V_{DD}=15V$, $V_{GS}=10V$, $I_{D}=1A$, $R_{GEN}=6\Omega$,	N		5		
-	•	R _{GEN} =0Ω, P-Channel	P N		2.8	1	nS
Turn-Off Delay Time	td(off)	V_{DD} =-15V, V_{GS} =-10V, I_{D} =-1A	P		53.6		
T. 11 (B)		$R_{GEN}=6\Omega$	N		3		
Fall-Time	t_{f}		P		46	 	

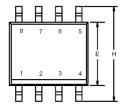
Notes

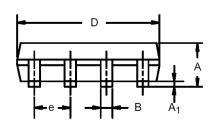
- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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Package Information

SO-8: 8LEAD





	MILLIN	IETERS	INCHES		
Dim	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	

